<u>WHAT IS CLAIMED IS:</u>

1. 1. A universal asynchronous receiver transmitter (UART) comprising:

2. a first-in, first-out (FIFO) buffer;

3. a circuit for detecting a last word transmitted from said FIFO buffer;

4. a transmitter empty circuit for generating a transmitter empty signal on a

5. transmitter empty control line when a last word transmitted from said FIFO buffer is

6. detected;

7. a delay circuit for delaying generation of said transmitter empty signal for

8. a programmable delay time; and

9. a programmable register for setting said programmable delay time.

1. 2. The UART of claim 1 wherein said transmitter empty signal is an

2. internal signal triggered from a stop bit of said last word.

1. 3. The UART of claim 1 wherein said programmable register comprises a

2. shadow register which is a write-only portion of a register only read by a user.

1. 4. The UART of claim 3 wherein said write-only portion comprises the

2. first 4 bits of a modem status register.

1. 5. The UART of claim 1 wherein said programmable register is a four bit

2. register.

1. 6. The UART of claim 1 further comprising:

2. a plurality of channels, each channel having said FIFO buffer, said circuit

3. for detecting a last word and said transmitter empty circuit; and

4. said delay circuit and said programmable register being a single circuit and

5. register connected to control the delay of said transmitter empty signal for each of said

6. channels.

1. 7. A universal asynchronous receiver transmitter (UART) comprising:

2. a first-in, first-out (FIFO) buffer;

3. a circuit for detecting a last word transmitted from said FIFO buffer;

4. a transmitter empty circuit for generating a transmitter empty signal on a

5. transmitter empty control line when a last word transmitted from said FIFO buffer is

6   detected, wherein said transmitter empty signal is an internal signal triggered from a stop

7   bit of said last word;

8   a delay circuit for delaying generation of said transmitter empty signal for

9   a programmable delay time;

10   a programmable register for setting said programmable delay time,

11   wherein said programmable register comprises a shadow register which is a write-only

12   portion of a register only read by a user;

13   a plurality of channels, each channel having said FIFO buffer, said circuit

14   for detecting a last word and said transmitter empty circuit; and

15   said delay circuit and said programmable register being a single circuit and

16   register connected to control the delay of said transmitter empty signal for each of said

17   channels.

1   8. The UART of claim 3 wherein said write-only portion comprises the

2   first 4 bits of a modem status register.

1   9. The UART of claim 1 wherein said programmable register is a four bit

2   register.

1   10. The UART of claim 7 further comprising at least 8 of said channels.